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Adiabatic pipelining: a key to ternary computing with quantum dots

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Abstract

The quantum-dot cellular automaton (QCA), a processing platform based on interacting quantum dots, was introduced by Lent in the mid-1990s. What followed was an exhilarating period with the development of the line, the functionally complete set of logic functions, as well as more complex processing structures, however all in the realm of binary logic. Regardless of these achievements, it has to be acknowledged that the use of binary logic is in computing systems mainly the end result of the technological limitations, which the designers had to cope with in the early days of their design. The first advancement of QCAs to multi-valued (ternary) processing was performed by Lebar Bajec *et al*, with the argument that processing platforms of the future should not disregard the clear advantages of multi-valued logic. Some of the elementary ternary QCAs, necessary for the construction of more complex processing entities, however, lead to a remarkable increase in size when compared to their binary counterparts. This somewhat negates the advantages gained by entering the ternary computing domain. As it turned out, even the binary QCA had its initial hiccups, which have been solved by the introduction of adiabatic switching and the application of adiabatic pipeline approaches. We present here a study that introduces adiabatic switching into the ternary QCA and employs the adiabatic pipeline approach to successfully solve the issues of elementary ternary QCAs. What is more, the ternary QCAs presented here are sizewise comparable to binary QCAs. This in our view might serve towards their faster adoption.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The pioneers in computer design were well aware that the world is not purely black and white. In this view, employing binary logic for its representation is not always the most suitable. Multi-valued logic, a generalization of binary logic, represents an important alternative. The potential advantages are greater data storage capabilities, faster arithmetic operations, better support for numerical analysis, non-deterministic and heuristic procedures, communication protocols, and efficient solving of non-binary problems [1–4]. Ternary logic is the simplest logic from the set of multi-valued logics, and the ternary number system offers the most efficient way of representing numbers [5]. Hence ternary logic seems quite a natural choice for multi-valued computer design. Unfortunately, all attempts at its realization have so far more or less fallen through, mostly due to the inaccessibility of basic building blocks compatible with multi-valued logic. On the other hand, bistable switches, above all the CMOS transistor, have made the construction of binary computers possible and simple. The absence of competitive multi-state building blocks has strengthened the dominance of binary technology, which can be noticed by observing the development guidelines for future processing platforms.

Nonetheless, we believe that with nanotechnology, which enables the manipulation of materials on the level of atoms, the time has come to reconsider the possibilities for the realization and usage of multi-valued logic. The initial work centred around the QCA platform employed for multi-valued processing, more precisely ternary logic, was performed by Lebar Bajec *et al* [6–8]. The authors have advanced the basic binary QCA cell (bQCA cell) originally introduced by

Lent *et al* [9] so that it allows the representation of three logic values and named it simply the ternary QCA cell (tQCA cell). The authors showed that the straight wire and the core of the inverter retain their functionality with a simple switch of the basic building block (i.e. the substitution of bQCA cells for tQCA cells promotes the two QCAs to work in a ternary domain). This, however, is not true for the corner wire and the fan-out. Besides that, extending the inverter core with a wire provokes erroneous behaviour. Even more problematic is the QCA, which implements ternary conjunction and disjunction, namely the majority voting gate [6–8, 10]. The authors did solve this issue, but by developing a more complex and from the size point of view suboptimal structure [7, 8]. Indeed, when compared to the binary counterpart, the QCA more than tripled in size. In addition, the new structure, although implementing both ternary conjunction as well as disjunction, does not allow input flexibility (i.e. using one as the selector of the computed function), which is one of the more highly praised features of the binary majority voting gate. This induces a concern that the new processing platform, due to the complexity of the primitives, which serve as building blocks of arithmetic-logic units and memorizing units, might experience a future similar to that of its predecessors.

In this paper we present solutions that are based on adiabatic pipelining [11], which is derived from adiabatic switching. The decision for its application originates from the benefits that were presented by researchers working on binary QCAs. The foremost two are increased switching stability of QCAs and simplified design of memorizing structures. A quantum-mechanics-based model with support for adiabatic switching was thus developed for modelling and simulation of tQCA cell based QCAs. The semi-classical model employed by Lebar Bajec *et al* is, due to its simplicity, easy to implement, but it allows only an overall estimation of the behaviour of tQCA based structures. Indeed a limited consideration of the quantum-mechanical properties removes the possibility of the introduction of adiabatic switching [12]. A quantum-mechanical model that is based on a Hubbard-type Hamiltonian with Coulomb repulsion, on the other hand, takes into account the full range of quantum-mechanical properties. By employing it here we present workable structures that implement the ternary corner wire, the ternary fan-out and the ternary majority voting gate and solve the interconnection problem of the ternary inverter.

In section 2 we present an overview of the ternary quantum-dot cell, followed by its quantum-mechanical description. In section 3.1 we describe the adiabatic pipelining and its influence on the quantum-mechanical model. Section 4 concludes by presenting tQCA cell based QCAs that employ adiabatic pipelining to implement the ternary inverter interconnection, the ternary corner wire, the ternary fan-out, the ternary symmetric inverter, and the ternary majority voting gate.

2. The ternary QCA

A quantum-dot cellular automaton (QCA) is a planar array of quantum-dot cells (also named QCA cells). Each cell contains a specific number of charges (typically electrons) and its influence on neighbouring cells is due to Coulomb interaction between its charges and the charges residing on them. Inside a single cell the charges reside only at designated locations, the quantum dots. They are able to tunnel between adjacent quantum dots, but tunnelling outside a cell is impossible. QCA cells operate at energy levels where Coulomb interaction prevails over tunnelling. This means that with specific planar arrays (arrangements) of QCA cells it is possible to mimic the behaviour of interconnecting wires as well as logic gates, and by interconnecting these, more complex devices capable of processing can be constructed.

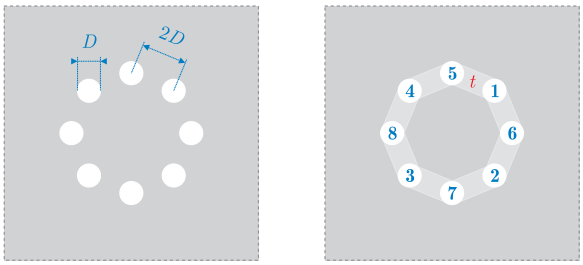


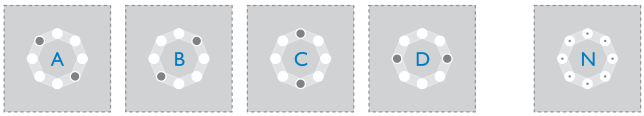
Figure 1. The geometry of the ternary quantum-dot cell presented by Lebar Bajec *et al* (a). The notation for the quantum dots and the tunnelling paths in the ternary quantum-dot cell (b).

The basic binary QCA, presented by Lent *et al*, is constructed from bQCA cells, which support the representation of binary information, and is capable of binary processing [9]. Its following advancement, the ternary QCA, presented by Lebar Bajec *et al*, employs tQCA cells, which support the representation of ternary information, and enables ternary processing [6].

2.1. The tQCA cell

The tQCA cell consists of eight circular quantum dots with diameter $D = 10$ nm. The quantum dots are arranged in a circular pattern with radius $D/\sin(\pi/8)$, so that the distance between neighbouring quantum dots equals $2D$ (see figures 1(a) and (b)). The tQCA cell contains two electrons, and the same tunnelling properties apply as in the bQCA cell (i.e. the electrons can tunnel only between adjacent quantum dots and not outside the cell). Since correct intercellular interaction is possible only if symmetric charge neutralization is ensured [13], a fixed positive charge of $\rho_+ = e_0/4$, where e_0 is the elementary charge, is assigned to each quantum dot.

In an isolated quantum-dot cell the contained electrons, due to Coulomb repulsion, strive to localize in quantum dots that ensure their maximal separation. In the tQCA cell there are four such arrangements (see figure 2(a)). According to Lebar Bajec *et al*, the arrangement with electrons in quantum dots 2 and 4 is marked as state A, and those with electrons in quantum dots 1 and 3 as B, 5 and 7 as C, and 6 and 8 as D. In the absence of external electric fields these four arrangements have exactly the same energy and correspond to the tQCA cell's ground state. This degeneracy manifests as an equally probable localization of the electrons in every dot, which is symbolically



a b

Figure 2. The four distinct electron arrangements, i.e. the four possible states marked A, B, C, and D, of a ternary quantum-dot cell, that correspond to the maximal interelectron separation (a) and the representation of a ternary quantum-dot cell in the neutral state (b).

represented as in figure 2(b). It is said that the tQCA cell is in a neutral state. The presence of external influences splits the degeneracy and causes one of the arrangements to become the tQCA cell's ground state.

One of the principles that define computing with QCAs is ground state computing [9]. It asserts that from the computing point of view the only acceptable state of a QCA cell is its ground state. The four possible electron arrangements of a tQCA cell can thus be interpreted as logical values. We here employ the balanced ternary logic, so state A is interpreted as logical value -1, state B as logical value 1, and states C and D as logical value 0. State D is typically, for reasons that will be explained in the following section, allowed only as an internal (processing) state [6–8].

Another principle which defines computing with QCA is edge driven computation. It asserts that the input cells, using which data are input into the QCA for processing, are typically situated at the borders of the structure and their states are fixed using external electrostatic fields. Similarly it asserts that the output cells, by means of which the processed data are output from the QCA, are positioned at the borders of the structure as well. Their states are read and interpreted as logical values, which represent the output of the logic function implemented by the QCA. The rest of the cells act as internal cells and are the only cells that perform any data transformation.

2.2. The model

For the tQCA cell we employ a simple model that uses a tight-binding Hubbard-type Hamiltonian similar to the one used by Lent *et al* for the bQCA cell. The quantum dots are represented as sites and the degrees of freedom internal to the quantum dots are ignored [9]. The corresponding Hamiltonian for the observed cell c is composed of four terms, and can be written as

$$\begin{aligned}\hat{H}^c = &\sum_{i,\sigma}(V_0 + V_i^c)\hat{n}_{i,\sigma} \\ &+ \sum_{i>j,\sigma} t_{i,j}(\hat{a}_{i,\sigma}^\dagger \hat{a}_{j,\sigma} + \hat{a}_{j,\sigma}^\dagger \hat{a}_{i,\sigma}) \\ &+ \sum_i E_Q \hat{n}_{i,\uparrow}\hat{n}_{i,\downarrow} \\ &+ \sum_{i>j,\sigma,\sigma'} V_Q \frac{\hat{n}_{i,\sigma}\hat{n}_{j,\sigma'}}{r_{i,j}}. \end{aligned} \tag{1}$$

The first term of equation (1) deals with the on-site energy, the second term accounts for electron tunnelling between sites, the third term is the on-site charging cost for localizing two electrons of opposite spin at the same site, and the last term corresponds to the Coulomb interaction between electrons localized at different sites. The number operator for site i and spin σ is represented by $\hat{n}_{i,\sigma} = \hat{a}_{i,\sigma}^\dagger \hat{a}_{i,\sigma}$, where $\hat{a}_{i,\sigma}^\dagger$ is the creation operator which creates an electron with spin σ at site i.

As we here consider a fixed number of electrons in the cell, the overall energy constant V_0 is irrelevant and is set to zero. The potential energy of an electron at site i in the observed cell c due to the existing charges in all other cells of the QCA is calculated as

$$V_i^c = \sum_{k\neq c,j} V_Q \frac{\rho_j^k - \rho_+}{r_{j,i}^{k,c}}, \tag{2}$$

where ρ_j^k is the electron density at site j in cell k, ρ_+ is the fixed positive charge used to maintain charge neutralization, $r_{j,i}^{k,c}$ is the distance between site j in cell k and site i in cell c, and V_Q is the Coulomb coupling strength. The on-site charging cost $E_Q = V_Q/(D/3)$ is a physically reasonable approximation for the Coulomb energy of two electrons separated by one third of the quantum dot's diameter D. The tunnelling energy $t_{i,j}$ is associated with tunnelling between dots i and j; the choice of its value will be explained in the following sections.

Although the QCA concept is generic in that there may be different possible implementations (e.g. metal-island, semiconductor, molecular, magnetic [14, 15]), the specific values of the physical parameters used here correspond to a semiconductor implementation based on a GaAs/AlGaAs material system [16, 17]. The choice has been made regardless of the known fabrication immaturity, primarily because the platform has been well investigated and the results obtained can easily be compared with their binary counterparts [18–21]. To be specific, the Coulomb coupling strength V_Q was evaluated for the GaAs/AlGaAs material system assuming a uniform dielectric constant of 11.9 [12], and its value is 120.9 meV.

To find the stationary states of the observed tQCA cell, we solve the time-independent Schrödinger equation

$$\hat{H}^c|\Psi_n\rangle = E_n|\Psi_n\rangle, \tag{3}$$

where $|\Psi_n\rangle$ is the nth eigenstate of the Hamiltonian and E_n is the corresponding eigenenergy. These eigenstates are found in the subspace of zero total spin projection,

$$|\Psi_n\rangle = \sum_{i,j} \psi_{ij}^n \hat{a}_{i,\uparrow}^\dagger \hat{a}_{j,\downarrow}^\dagger |0\rangle, \tag{4}$$

where $\hat{a}_{i,\uparrow}^\dagger \hat{a}_{j,\downarrow}^\dagger|0\rangle$ represents spin-up and spin-down electron states at sites i and j, respectively, and the summations run over all eight sites in the cell. The Hamiltonian matrix is diagonalized numerically using realistic parameters corresponding to GaAs/AlGaAs.

2.3. Mapping tQCA cell states to logical values

In order to provide the means for processing every processing platform must use some sort of mapping from physical quantities into logical values and vice versa. The classical

CMOS uses voltage levels; the binary QCA, on the other hand, uses polarization [9]. As a convenient single variable measure the polarization enables mapping of a bQCA cell state into the corresponding logical value, and assuming an ideal charge distribution also vice versa. The polarization presented by Lent *et al* is, however, not directly applicable to tQCA cell states; therefore we characterize the logical value of the cell by the probability that the corresponding logical state S (A, B, C, or D) is occupied.

The ground state of the system is, in our case due to the strong repulsive interaction, always being a spin singlet. The logical states are thus represented by singlet pairs (dimers) of electrons occupying two diametrical sites, $|\mathsf{A}\rangle = \frac{1}{\sqrt{2}}(\hat{a}^{\dagger}_{2,\uparrow}\hat{a}^{\dagger}_{4,\downarrow} - \hat{a}^{\dagger}_{2,\downarrow}\hat{a}^{\dagger}_{4,\uparrow})|0\rangle$ for $\mathsf{S} = \mathsf{A}$, for example, and correspondingly for other states presented in figure 2. An appropriate quantifying measure, if the system is in a particular state S, is the density–density correlation function

$$P_{\mathsf{S}} = \sum_{\sigma,\sigma'} \langle \Psi_0 | \hat{n}_{i,\sigma} \hat{n}_{j,\sigma'} | \Psi_0 \rangle, \tag{5}$$

where i and j are sites characterizing the logical state S. In our case of negligible double occupancy P_{S} simplifies to the probability that electrons are in quantum state $|\mathsf{S}\rangle$, i.e., $P_{\mathsf{S}} = |\langle \mathsf{S}|\Psi_0\rangle|^2$.

In the case of a static charge distribution or in the limit when electron density fluctuations are negligible, the correlation function decouples, $P_{\mathsf{S}} = \rho_i \rho_j$, where the electron density ρ_i is given by

$$\rho_i = \sum_{\sigma} \langle \Psi_0 | \hat{n}_{i,\sigma} | \Psi_0 \rangle. \tag{6}$$

In our approach the electron density is also applied to represent the charge density in equation (2).

The logical value of the cell can also be characterized by a single parameter L, which takes values $L = \pm 1$ if the cell is in logical states A or B, respectively, and $L = 0$ if the cell is in logical states C or D. A suitable choice is

$$L = \frac{P_{\mathsf{B}} - P_{\mathsf{A}}}{Q}, \tag{7}$$

where $Q = P_{\mathsf{A}} + P_{\mathsf{B}} + P_{\mathsf{C}} + P_{\mathsf{D}}$ is the probability that the ground state of the cell is in one of the quantum states $|\mathsf{S}\rangle$. Such a single measure L is reliable under the condition that Q is sufficiently close to unity—fulfilled in the regime of strong Coulomb repulsion studied in this paper—and deviations occur only during transitions between the states.

3. The cell to cell interaction

QCA processing is based on cell to cell interaction, where the state of a cell influences the states of its neighbours and vice versa. The basic interaction shown in figure 3 comprises two tQCA cells, where cell X acts as the input (driver) and cell Y as the observed output. We choose the cells' centres to be separated by $r = 110$ nm, so that the proportion between the maximal interdot distance in a cell and the intercell distance remain the same as in the case of the bQCA cell.

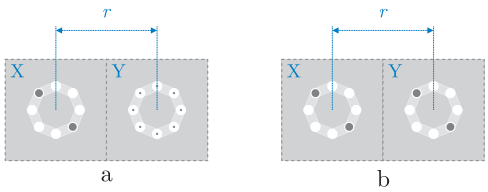


Figure 3. The tQCA cell to cell interaction; the initial state, where cell X is in state A and cell Y is neutral (a), and the resulting state, where cell Y assumes state A (b).

The model, equation (1), can easily be solved for a single cell. However, to analyse a QCA composed of a larger number of tQCA cells in the same way would soon reach the boundaries of feasibility. Indeed, exact diagonalization methods become intractable as the number of cells and the number of basis states increase rapidly (e.g. a site-ket basis for a QCA composed of k tQCA cells requires 64^k ket vectors). To overcome this problem when modelling QCAs composed of bQCA cells, Lent *et al* proposed a method called the intercellular Hartree approximation (ICHA) [22]. Here we employ the same technique. The ground state of the entire system (i.e. the QCA) is found by iteratively solving for the ground state of each cell. A single cell is observed using (3) and the effects of that cell on the potential energies in all other cells are then updated. The intercellular interaction is treated self-consistently using the Hartree approximation.

The cell response function is obtained by applying a static charge distribution (ρ_i^{D}) to cell X and observing the resulting charge distribution in cell Y. As a series of sequential steps first a transition from one ground state to neutral and then from the neutral state to another ground state is applied to cell X. The static charge distribution for the transition from the neutral state to a ground state is computed as (see figure 4)

$$\begin{aligned} \rho_i^{\mathrm{D}}(s) &= \sqrt{s(1-\rho_+)^2 + \rho_+^2}, \\ \rho_{i'}^{\mathrm{D}}(s) &= \min(\rho_+, (1-\rho_i^{\mathrm{D}}(s))/2), \\ \rho_{i''}^{\mathrm{D}}(s) &= 1 - \rho_i^{\mathrm{D}}(s) - 2\rho_{i'}^{\mathrm{D}}(s), \end{aligned} \tag{8}$$

where $s \in [0, 1]$. With $s = 0$ the static charge distribution gives a neutral cell, whereas with $s = 1$ a cell with electrons occupying two diametrical quantum dots is obtained. The charge density in quantum dots characterizing the ground state is given by $\rho_i^{\mathrm{D}}(s)$, (i.e. $i = 2$ and 4 for ground state A, 1 and 3 for ground state B, etc). The charge density in the nearest-neighbour quantum dots is given by $\rho_{i'}^{\mathrm{D}}$ (i.e. $i' = 5$, 6, 7, and 8 for states A and B, etc.) and the charge density in the next-nearest-neighbour quantum dots is given by $\rho_{i''}^{\mathrm{D}}$ (i.e. $i'' = 1$ and 3 for state A, etc.).

Figure 5 presents six state transitions of cell X and the corresponding response functions for cell Y. Every transition of cell X was carried out in 2000 steps. The results were obtained using the ICHA approach for tunnelling energy $t = -0.01$ meV. Reverse transitions are not presented as they are symmetrical to those presented. For each transition there are four graphs depicting the P_{S} for states A, B, C, and D. The lighter curve (blue) is for cell X and the darker curve (orange)

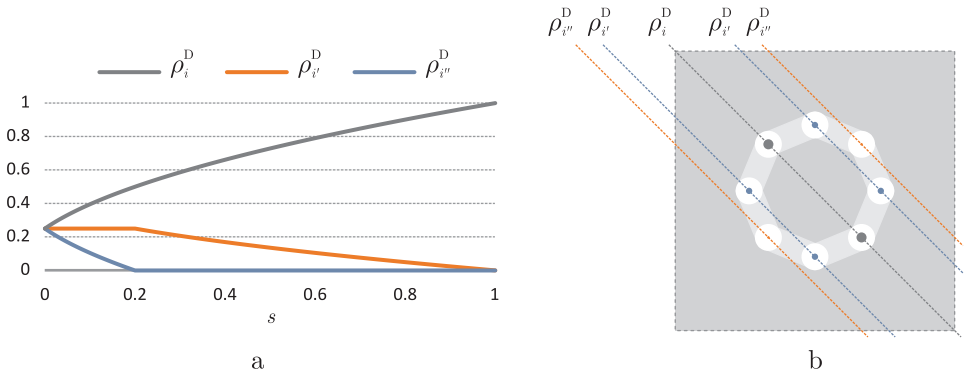


Figure 4. Plot of the static charge distribution (a) applied to cell X for the transition from the neutral state to state A (b).

is the response of cell Y. On observing the graphs, it can be noticed that cell Y follows the state changes of cell X. What is more, cell Y saturates very quickly to the corresponding state and the response function is highly nonlinear for the initial and final states and almost flat for the other two. As in the case of the bQCA cell [23], the abruptness of the response function depends on the ratio of tunnelling energy to the Coulomb energy for electrons on neighbouring sites.

3.1. Adiabatic pipelining

In computer science, pipelining is a well known technique, typically used for improving computing performance [24]. The basic idea is to divide a problem into independent subproblems, which can be worked on simultaneously, but in sequence. From this viewpoint, pipelining is similar to an assembly line in a manufacturing plant. New inputs are accepted at one end, are worked on in a sequence of stages, and are output at the other end of the assembly line. By laying out the production process on an assembly line, products at various stages can be worked on concurrently. In computer science, a pipeline refers to a set of processing elements, namely stages, connected in a series in which the output of one stage provides the input to the next one. Each stage is dedicated to solving a particular independent subproblem and can be executed in parallel with the other stages. To overcome synchronization problems the execution of stages is usually controlled by one or more clock signals. Using pipelining, the computing performance is improved by the increase of the system's throughput when processing a stream of data.

In QCAs, the pipeline architecture was introduced by Lent *et al* [11]. Interestingly enough, it was not used primarily due to the above-described benefits, but to increase the processing reliability of complex QCAs. The latter mainly depends on the reliability of the switching process, i.e. the transition from a cell's ground state that represents one logical value to a ground state that represents another. An uncontrolled execution of this transition is called abrupt switching, while a controlled execution is achieved by applying the concept of adiabatic switching [11]. Its implementation in QCAs is based on a cyclic control signal, denoted as the adiabatic clock, which, by means of an electric field that acts on the interdot barrier heights, controls the probability of tunnelling of electrons within a QCA cell. The adiabatic clock signal is composed of four phases (see figure 6). The gradual increase of barrier heights is called the switch phase (S) and it serves the affected cells' gradual update of their states with respect to states of their neighbours. The phase with constant and raised barriers is called the hold phase (H) and is intended for the stabilization of the cells' states when they are to be transmitted to the neighbours that are in the switch phase (i.e. the affected cells act as a fixed input for all other cells). The gradual decrease of the barrier heights and the constant and lowered barriers are called release (R) and relax (L) respectively, and they support the cells' gradual preparation for a new switch (i.e. the cells' states gradually transit to a neutral state).

In the Hamiltonian presented in equation (1) the interdot barrier height is modelled through parameter t, which is thus directly affected by the adiabatic clock signal. For the tQCA cells the chosen clock signal is not linear, as it turned out to be too abrupt for proper localization of the electrons. In fact when raised barriers correspond to 0 meV and lowered to -2 meV, preliminary tests showed that most of the 'action' happens when $t \in [-0.5, 0]$ meV [25]. The increased number of quantum dots with respect to the bQCA cell leads to more possible locations for the electrons to tunnel to; hence their localization in the desired quantum dots is possible only when the barriers are sufficiently high. The adiabatic clock signal for the tQCA cell is thus based on a sinusoidal function that has been scaled to the interval [0, 1] (see figure 6). After dividing the function into two sections, one monotonically increasing and the other decreasing, we choose the first section as the control signal in the switch phase and the second as the control signal in the release phase. The hold and relax phases are kept constant: the former with barriers raised and the latter with barriers lowered. The constructed signal has a gradual change in the vicinity of raised barriers and thus allows more time for the electrons to successfully localize in the appropriate quantum dots.

It is desired that the number of cells being controlled by one signal is as large as possible, as this reduces the challenges that would be caused by attempting to deliver a separate clock signal to every cell. Nevertheless, increasing the number of cells controlled by one adiabatic clock diminishes the reliability of the switching process; hence a compromise is often the only option. The adiabatic clock, however,

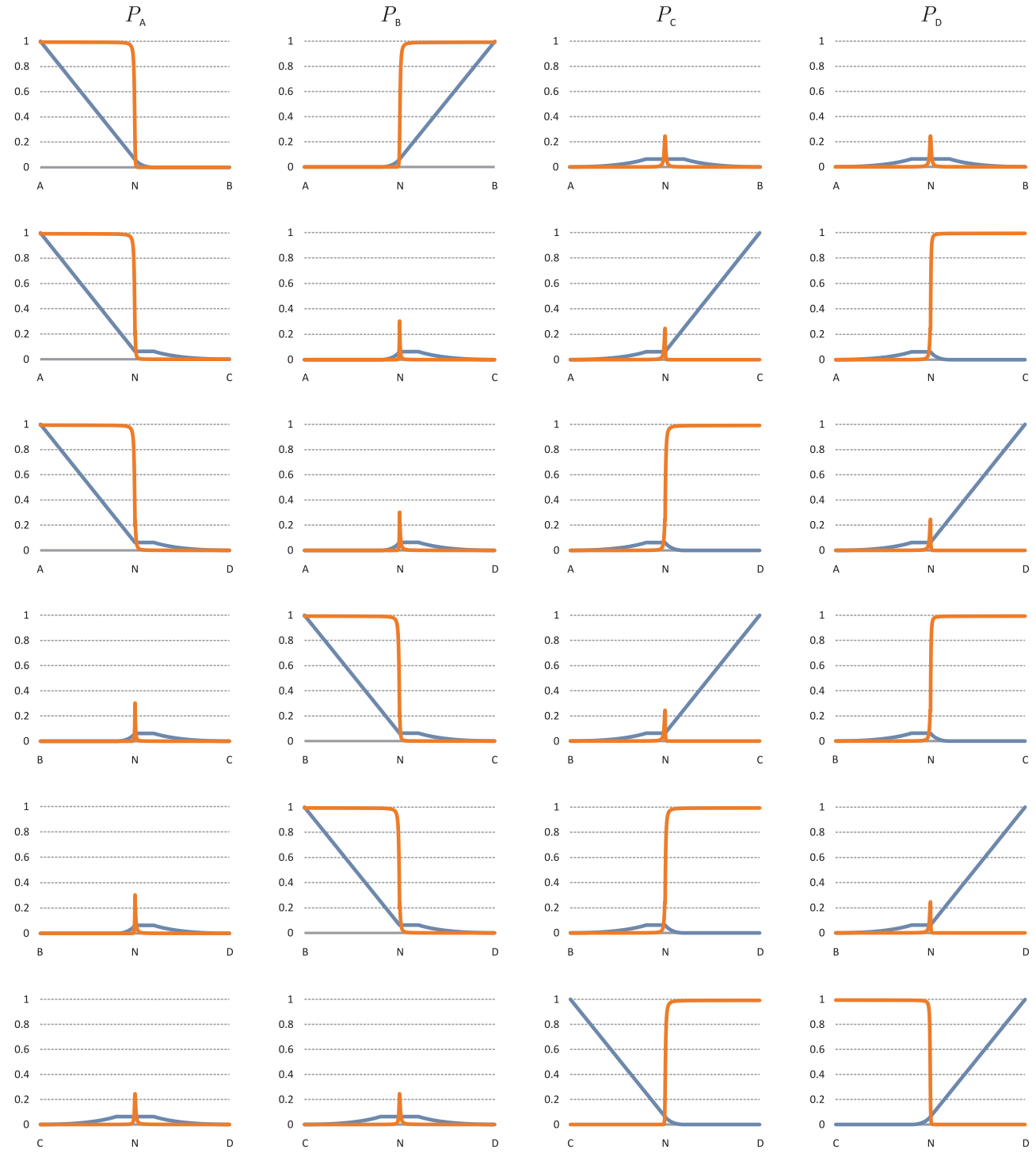


Figure 5. The cell response functions for six state transitions. The lighter curve (blue) denotes the state transition of cell X and the darker curve (orange) denotes the response function of cell Y.

enables the introduction of the pipeline architecture. Since the clock signal is composed of four phases, any QCA can be decomposed into smaller stages or subsystems controlled by four phase shifted signals, each defining its own clocking zone (see figure 7). Let C_0 denote the base signal (as presented in figure 5) and C_i, $i = \{0, 1, 2, 3\}$ the base signal phase shifted by i phases. The phase shifted nature of the controlling signals allows the stages that are in the hold phase to act as inputs for stages that are in the switch phase (see figure 7). Therefore a subsystem after performing the computation can be designed to lock its state and act as the input for another subsystem. As the transaction is finished the second subsystem can start processing while the first subsystem is ready for processing on new inputs.

4. Elementary ternary QCAs

We have simulated the basic ternary primitives (wire, inverter, and AND/OR logic gate) presented by Lebar Bajec *et al*

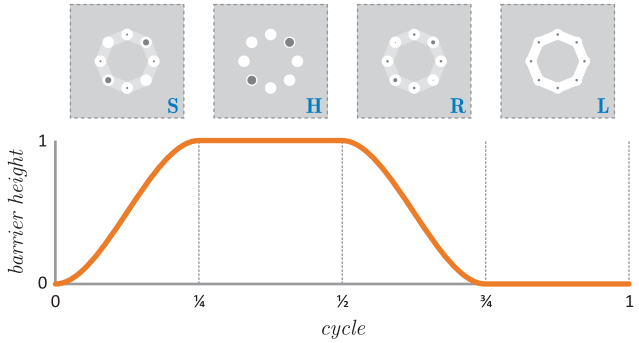


Figure 6. The adiabatic clock signal, which controls the cells' switching process, is composed of four phases, namely: switch (S), hold (H), release (R), and relax (L). In the graph the barrier height is normalized to the interval [0, 1], where value 0 denotes lowered barriers (high probability of the electrons tunnelling between adjacent quantum dots) and value 1 denotes raised barriers (no tunnelling of electrons possible).

in [7] under abrupt switching with a tunnelling energy of $t = -0.01$ meV. The results obtained have been compared with those presented by Lebar Bajec *et al*, and for the problematic structures new pipelined architectures are proposed.

4.1. The inverter

Lebar Bajec *et al* have focused their research foremost on the ternary inverter core (figure 8(a)). The results the authors obtained show that the proposed implementation behaves correctly. Simulations based on our quantum-mechanical model confirm their claims. Indeed, the balanced ternary logic negation can be expressed as

$$y = \overline{x} \equiv -x, \tag{9}$$

where $x, y \in \{-1, 0, 1\}$; then if logical value x corresponds to the state of input cell X and logical value y to the state of output cell Y it can be seen that the QCA acts as a ternary inverter (see the truth table in figure 8).

In order to construct more complex structures, the inverter core has to be connected to other primitives. This is achieved by means of wires. Simulations based on our quantum-mechanical model show that the interconnection of a wire to the input section of the inverter core does not affect its behaviour even when abrupt switching is employed (see figure 8(b)). On the contrary, the interconnection of the inverter

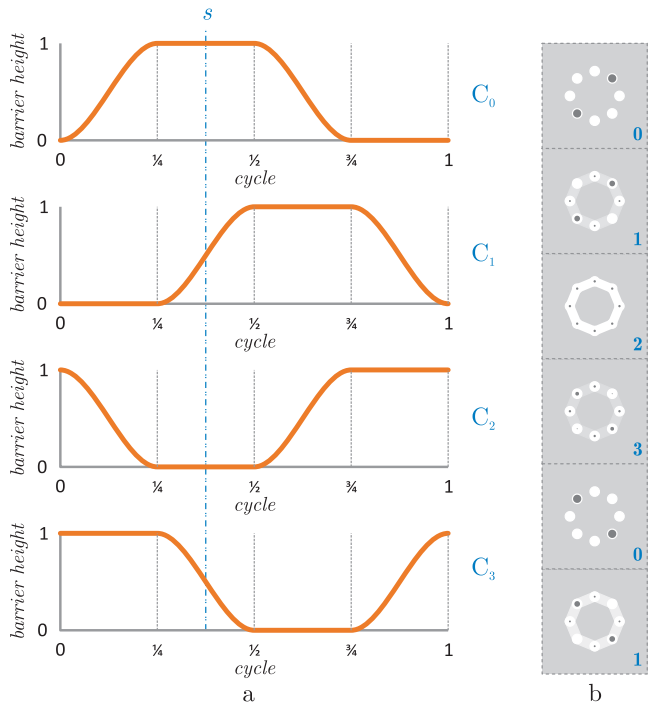


Figure 7. Four phase shifted adiabatic clock signals (a) and an example of the adiabatic pipeline architecture applied to the ternary wire QCA (b). The wire is decomposed into six stages (subsystems) controlled by four signals. This achieves synchronization of data flow from top to bottom. The figure shows a snapshot (marked *s* in the signal graphs) from a sequence of data transfers along the wire. The first and fifth cells are in the hold phase and serve as fixed inputs for the second and sixth cells, which are in the switch phase, respectively. It can be noticed that due to the pipeline architecture they can hold different data at the same time instant. The third cell is in the release state and the fourth cell is relaxed, so their influence on the data being transferred is minimal.

core's output section to a wire is more problematic, resulting in highly unstable behaviour, which mostly favours the output state C. The issue can be solved by treating the inverter as a pipeline of two or three stages. In the first case the input wire and inverter core are assigned to one clocking zone (controlled by signal C_0) and the output wire to another clocking zone (controlled by signal C_1), as in figure 9. In the second case the input QCA wire is controlled by signal C_0, the inverter core by signal C_1, and the output wire by signal C_2. In order to maintain a simple clocking scheme the two-stage solution is preferred.

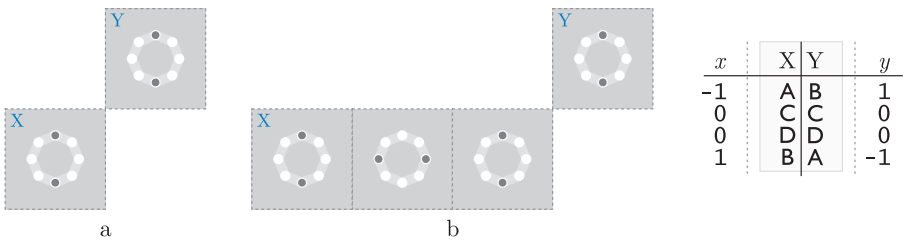


Figure 8. The core of a ternary inverter (a) and the extension of the input section (b). The behaviour matches the truth table of ternary negation.

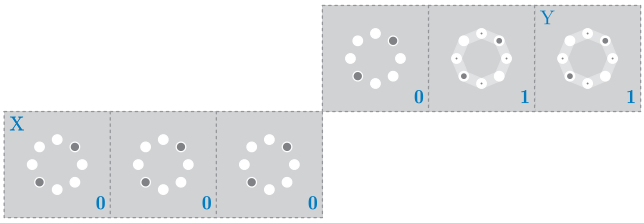


Figure 9. The solution of the inverter interconnection issue by using two pipeline stages.

4.2. The corner wire and fan-out

Our analysis shows that the ternary wire behaves correctly as long as the tQCA cells are aligned in a straight line. The presence of a corner in a wire or a fan-out yields erroneous behaviour, as presented in figure 10. Both structures result in erroneous output whenever the input state is A or B. The problem arises from the conflicting situation in the cell to cell interaction at the corner section of the QCA. For example, while observing the behaviour of the corner wire (see figure 10(a)) during the transmission of state A (or B) from input cell X to output cell Y it is expected that the second cell seizes the state of the input cell and this should force the same state to the third cell. The fourth cell, however, has a conflicting situation. It is expected to seize the third cell's state, but due to their diagonal arrangement it is also expected to seize the inverted state of the second cell. The conflicting influence of the second and third cell prevents the fourth cell from occupying the desired state and causes the electrons to favour localizing in quantum dots 6 and 8 (i.e. state D), thus achieving the maximal separation with the electrons in the other two cells. This has a reflux effect on the third and consequently the second cell as well as transmission to the output cell. The end result is an erroneous processing output. The transmission of states C and D over the corner wire behaves as expected, because the states are alternating along the wire, which ensures that the electrons in cells two, three, and four are arranged so that their maximal spatial separation is achieved even from the cell to cell point of view, and no conflicting situation emerges. A similar scenario occurs in the case of the fan-out (see figure 10(b)). In the section where the wire splits there are four cells in a conflicting situation. It is important to note that the above-described scenario takes place if abrupt switching is used as well as when all cells are subjected to the same adiabatic clock signal.

The corner wire and fan-out issue can be easily solved using the pipelining concept. As discussed, the issue originates from the conflicting situation of the corner cells. It can be solved by splitting the QCA into two subsystems (stages), controlled by two phase shifted clock signals C_0 and C_1 (as depicted in figure 11). Concentrating on the corner line, this decomposition is designed so as to fix the state of cells two and three and thus prevent the reflux effect from happening. Moreover, it ensures the desired behaviour of cell four. The latter is due to the larger influence of cell three than that of

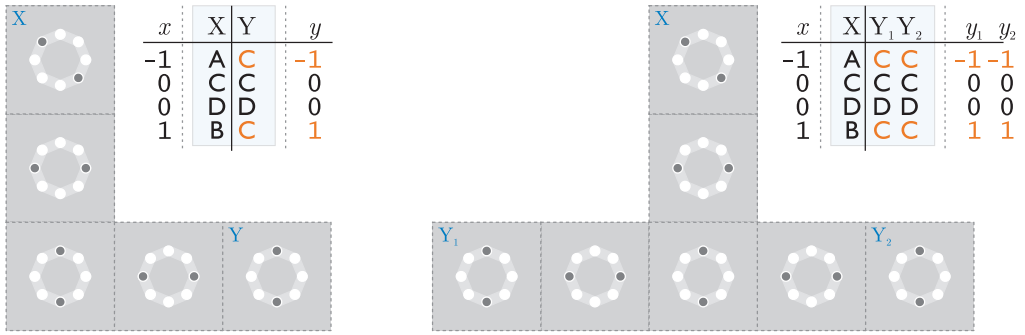


Figure 10. The corner wire and fan-out and their erroneous behaviour.

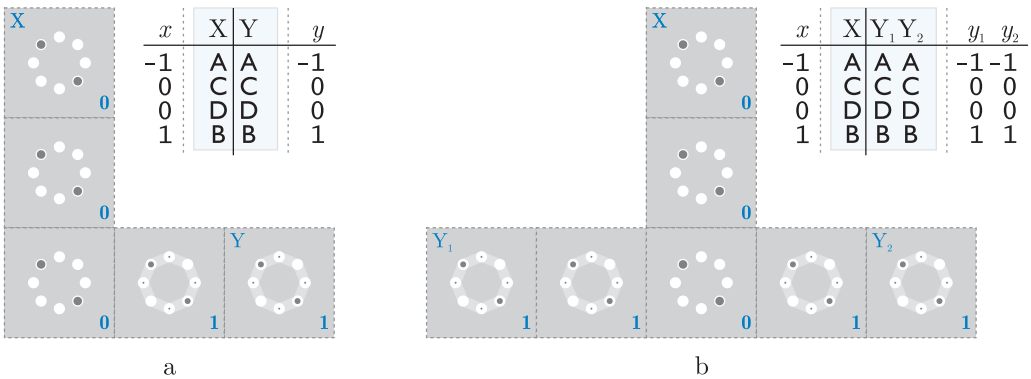
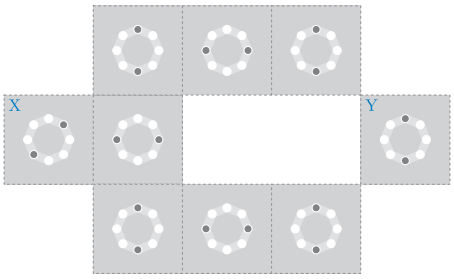
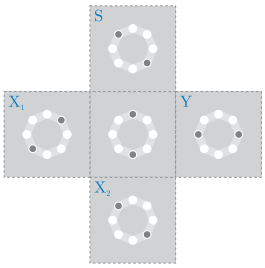


Figure 11. The pipeline architecture of corner wire and fan-out enables their correct behaviour.



x	X	Y	y
-1	A	C	1
0	C	C	0
0	D	D	0
1	B	C	-1

Figure 12. The erroneous behaviour of the symmetric ternary inverter.



	x_1	x_2	S	X_1	X_2	Y	y
AND(x_1,x_2)	-1	-1	A	A	A	A	-1
	-1	0	A	A	C	A	-1
	-1	1	A	A	B	A	-1
	0	-1	A	C	A	A	-1
	0	0	A	C	C	C	0
	0	1	A	C	B	C	0
	1	-1	A	B	A	D	-1
	1	0	A	B	C	C	0
	1	1	A	B	B	B	1
OR(x_1,x_2)	-1	-1	B	A	A	A	-1
	-1	0	B	A	C	C	0
	-1	1	B	A	B	D	1
	0	-1	B	C	A	C	0
	0	0	B	C	C	C	0
	0	1	B	C	B	B	1
	1	-1	B	B	A	B	1
	1	0	B	B	C	B	1
	1	1	B	B	B	B	1

Figure 14. The QCA obtained by simple substitution of bQCA cells for tQCA cells in the binary majority voting gate and the corresponding truth table. When obeying the preconditions about the selector input S and the state D the QCA gives only two erroneous outputs.

cell two. As both of these have electrons fully localized with no probability of their tunnelling, cell four seizes the state of cell three. From the pipeline point of view this can be described as bringing the correct state to the corner and only then taking it towards the other (one or two) directions. Note, however, that if the corner cell (cell three) is not designated to the clocking zone controlled by signal C_0 the behaviour is incorrect, as if without adiabatic pipelining applied.

4.3. The symmetric inverter

In binary QCAs the shortcomings of the inverter discussed in section 4.1 are elegantly solved by a symmetric inverter. The latter, however, does not suffice in the ternary QCA case. A thorough analysis (see figure 12) shows that the problem arises from the inverter's mid-section, which comprises a fan-out and two corner wires (one above and one below). As was demonstrated in the previous section, the two structures exhibit erroneous behaviour whenever they are controlled by a single adiabatic clock signal. Following the methodology of their amendment, the symmetric ternary inverter can be split into three stages (see figure 13(a)). The input section of the fan-out is assigned to clocking zone 0 controlled by signal C_0, and the output section of the fan-out and the input section of the corner wire are assigned to clocking zone 1 (signal C_1), while the inverter core is assigned to clocking zone 2 (signal C_2). The proposed clocking scheme can be further simplified by combining the second and third stages into a single one controlled by signal C_1. The two-stage QCA obtained (see figure 13(b)) produces correct results, although in a rather unusual way. More specifically, in the case of input states C and D the symmetric ternary inverter behaves as expected. Input states A and B yield the correct output states as well (B and A correspondingly), but, as a contrast to the three-stage solution, for input state A the 'expected' state transfer is carried out only over the upper data path, whereas for input state B the transfer is only over the lower data path (see figure 13(b)).

4.4. The majority voting gate

The QCA called the majority voting gate, or shorter majority gate, is one of the best assets of binary QCAs. The structure is expected to provide as the output state the state that is present at the majority of the inputs. Besides its architectural simplicity, one of the most praised features is its ability to perform logic AND and logic OR operations, achieved simply by fixing one of the input cells to the corresponding state. Lebar Bajec *et al* tried to preserve these properties in the ternary domain as well by using the same QCA but substituting bQCA cells for tQCA cells [6–8]. To solve the problems that have emerged the authors introduced two preconditions. The first states that only the input cell denoted as S can be used as the selector of the gate's behaviour, whereas inputs X_1 and X_2 can serve only as inputs to the selected logic function (see figure 14). The second states that state D is allowed only as an internal state; thus it cannot be used on any of the inputs.

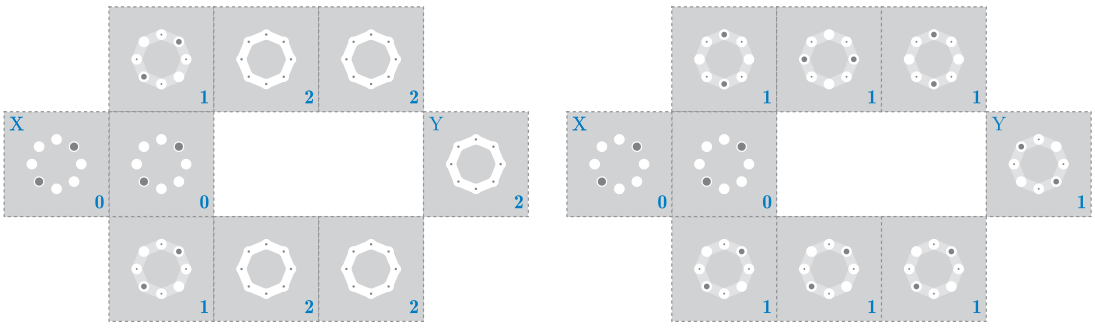


Figure 13. Two possible pipeline architectures of the symmetric ternary inverter: a three-stage (a) and a two-stage (b) implementation.

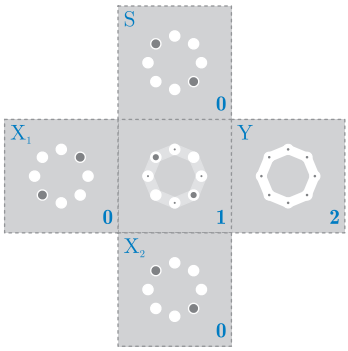


Figure 15. The three-stage pipeline architecture of the ternary majority voting gate.

The ternary logic functions AND and OR can be expressed in general multi-valued logic form as

$$y = \mathrm{AND}(x_1, x_2) \equiv \min(x_1, x_2),$$
$$y = \mathrm{OR}(x_1, x_2) \equiv \max(x_1, x_2), \tag{10}$$

where $x_1, x_2, y \in \{-1, 0, 1\}$. Using x_1, x_2, and y as the logic values corresponding to states of input cells X_1 and X_2 and output cell Y, the behaviour of the QCA, when obeying the two preconditions, complies almost completely with the ternary AND and OR logic functions. Indeed the truth table reveals only two erroneous output states: $\mathrm{OR}(-1, 1) = \mathrm{AND}(1, -1) =$ D (see figure 14). In [7], Lebar Bajec *et al* presented a QCA composed of three majority voting gates, which implements the ternary AND and OR logic functions completely. However, in view of the number of required cells, it is quite space consuming. Indeed, even when disregarding interconnections of the individual majority voting gates, the number of required cells tripled with respect to the binary QCA.

Following the idea of adiabatic pipelining we here present two QCAs constructed by using the same number of cells as for the binary majority gate, which as a bonus allow input flexibility (i.e. each of the three inputs can be chosen as the selector of the QCA's behaviour).

The first continues with the basic idea of Lebar Bajec *et al*, i.e. it is directly derived from the binary majority voting gate by simple substitution of bQCA cells for tQCA cells, thus preserving the architecture of the binary majority voting gate. A thorough analysis of the QCA's behaviour using the quantum-mechanical model revealed that a possible source for invalid outputs is the cornering relation of the three inputs. The only two invalid output states are generated when the three inputs are symmetrical; in states A, B, A or B, A, B, respectively.

The solution's concept is thus to first compute the intermediate result and only then transfer it to the output cell. More precisely, first compute the minimum of the remaining two inputs when the third is in state A and the maximum when it is in state B and then safely transfer this value to the output cell [25]. The approach can be easily implemented using a three-stage pipeline architecture (see figure 15). The input cells are assigned to clocking zone 0 (i.e. controlled by signal C_0), the internal cell to clocking zone 1 (signal C_1), and the output cell to zone 2 (signal C_2). This ensures that when the inputs are in the hold phase the internal cell is in the switch phase (i.e. slowly transiting to a state that is in accordance with the states of all three inputs) and the output cell is in the relaxed phase. When the internal cell is in the hold phase the output cell is in the switch phase, whereas the input cells are in the release phase. This ensures that during the output cell's highest 'activity' the influence of the input cells will be minimal (in fact their states will be close to neutral).

Table 1. The full range of possible input states and the resulting outputs for the pipelined ternary majority voting gate. The lighter marked (orange) outputs represent erroneous output cell states. Note, however, that these occur only when states C and D are applied as inputs simultaneously.

S	X_1	X_2	Y	S	X_1	X_2	Y	S	X_1	X_2	Y	S	X_1	X_2	Y
A	A	A	A	B	A	A	A	C	A	A	A	D	A	A	A
A	A	C	A	B	A	C	C	C	A	C	C	D	A	C	A
A	A	D	A	B	A	D	D	C	A	D	A	D	A	D	D
A	A	B	A	B	A	B	B	C	A	B	C	D	A	B	D
A	C	A	A	B	C	A	C	C	C	A	C	D	C	A	A
A	C	C	C	B	C	C	C	C	C	C	C	D	C	C	C
A	C	D	A	B	C	D	B	C	C	D	C	D	C	D	D
A	C	B	C	B	C	B	B	C	C	B	C	D	C	B	B
A	D	A	A	B	D	A	D	C	D	A	A	D	D	A	D
A	D	C	A	B	D	C	B	C	D	C	C	D	D	C	D
A	D	D	D	B	D	D	D	C	D	D	D	D	D	D	D
A	D	B	D	B	D	B	B	C	D	B	B	D	D	B	D
A	B	A	A	B	B	A	B	C	B	A	C	D	B	A	D
A	B	C	C	B	B	C	B	C	B	C	C	D	B	C	B
A	B	D	D	B	B	D	B	C	B	D	B	D	B	D	D
A	B	B	B	B	B	B	B	C	B	B	B	D	B	B	B

A thorough inspection of the truth table (table 1), while maintaining the precondition about state D, reveals that the QCA now behaves as a ternary majority voting gate. The output reflects either the state that has been present at the majority of the inputs or state C if the majority cannot be determined (e.g. in the case of input combination A, B, C). Further analysis reveals that, due to this, the choice for the selector of the gate's behaviour is not limited solely to input cell S, but the ternary majority voting gate computes the ternary AND between the remaining two inputs whenever the third is in state A and ternary OR whenever it is in state B.

When designing complex structures the restriction of state D being allowed only as an internal state limits wires to odd lengths, and this might at times prove to be quite challenging. The pipelined ternary majority voting gate, as a plus, behaves correctly even when this precondition is not obeyed. Indeed, if one follows the initial logical value assignment (i.e. state D is logical value 0) the QCA gives the correct output even if state D is used as the input state. There is, however, one restriction: states C and D must never appear as inputs simultaneously. The described feature simplifies the design, as wires of arbitrary length can be used as long as the lengths of interconnections to the three inputs of the pipelined majority voting gate are all odd or even.

Although the described QCA proves successful it uses a three-stage clocking scheme, which could potentially introduce the adiabatic clock signal wiring problem that could easily destroy the advantages gained by the local interconnectivity and the pipelined architecture. Research performed by Tahoori *et al* showed that the binary majority voting gate

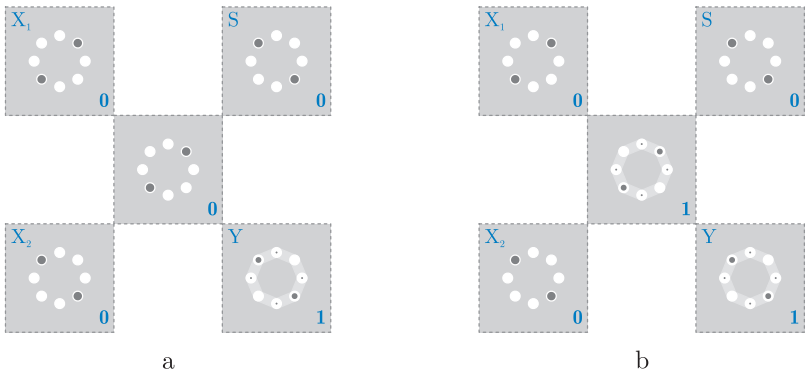


Figure 16. The two adiabatic pipeline implementations of a diagonal ternary majority voting gate.

implemented using 45° rotated cells (i.e. as a crossing of three 45° wires) results in a more fault-tolerant QCA [26]. The ternary counterpart was obtained using the same design philosophy as before, i.e. by substitution of bQCA cells for tQCA cells. For the tQCA cell there is no advantage when rotating it by 45°; however, a similar effect (i.e. alternating states A and B) can be achieved with a diagonal arrangement of cells. Although the obtained QCA under abrupt switching (or single clocking zone adiabatic switching) shows erroneous behaviour, its true advantage is manifested when a pipeline architecture is applied. Indeed, its robustness diminishes the number of required pipeline stages to two, thus simplifying the clocking scheme. There exist two possible implementations. The first (see figure 16(a)) uses signal C_0 to control the input cells as well as the internal cell and signal C_1 to control the output cell. This way the QCA begins by computing the state, which equals the inverse of the state representing the majority of the states present on the three inputs, all in the process while the inputs are still being applied, and only afterwards is the inverse of this value transmitted to the output cell. The second implementation (see figure 16(b)) again designates the input cells to clocking zone 0 (controlled by signal C_0), but designates the internal and output cell to clocking zone 1 (signal C_1). This allows the fixing of the inputs followed by the computation of the intermediate result and the state present at the majority of the inputs simultaneously. Needless to say, the resulting behaviour is the same as in the case of the three-stage pipelined majority voting gate. Therefore we denote this QCA as a *pipelined diagonal majority voting gate*.

5. Conclusion

This paper presents the basic architectural guidelines for the design of ternary quantum-dot cellular automaton (QCA) based processing elements. It shows that the introduction of an adiabatic pipeline can successfully solve the problems related to the architecture of elementary ternary logic QCAs, i.e. the corner wire, the fan-out, the inverter, and the majority voting gate. The assignment of appropriate clocking zones can be further used to simplify the clocking scheme and thus diminish the challenges related to adiabatic clock signal interconnection. What is more, the architectures of the proposed QCAs equal those employed for the implementation of the corresponding binary logic functions. This opens up the possibility of using design rules similar to those developed for the binary QCA domain. Our current research is focused on the development of ternary QCAs that implement a functionally complete set of ternary logic functions. These shall represent the key building blocks of advanced ternary arithmetic-logic and memorizing units, the principal components of ternary processors. It should also be noted that our numerical results rely on quantum-mechanical calculations based on realistic parameters appropriate for GaAs/AlGaAs, but we are well aware of the implementation problems in possible realization of operational devices, and for this reason the switching dynamics and material suitability are also part of our ongoing research.

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